08-23-00

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Tongbi Jiang et al.
Title: CIRCUIT BOARD
Attorney Docket No.: 303.705US1

PATENT APPLICATION TRANSMITTAL

BOX PATENT APPLICATION
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Washington, D.C. 20231

We are transmitting herewith the following attached items and information (as indicated with an "X"):

X Return postcard.
X Utility Patent Application under 37 CFR § 1.53(b) comprising:
- X Specification (17 pgs, including claims numbered 1 through 44 and a 1 page Abstract).
- X Formal Drawing(s) (4 sheets).
- X Signed Declaration (3 pgs).
- X Check in the amount of $2,214.00 to pay the filing fee.

X Assignment of the invention to Micron Technology, Inc. (3 pgs) and Recordation Form Cover Sheet.
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[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED				$0.00
BASIC FEE				$690.00
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CIRCUIT BOARD

Field of the Invention

This invention relates to circuit boards, and more particularly, to increasing circuit board reliability.

Background of the Invention

Printed circuit boards, which are used in the manufacture of electrical, mechanical, electro-mechanical, and other kinds of products, provide a substrate for mounting a die on which integrated circuits, such as processors, memories, and amplifiers, are fabricated. Figure 1 shows a cross-sectional view of a prior art ball-grid array (BGA) package 100 which includes printed circuit board 103 coupled to board 105 by solder balls 107, and die 109 coupled to printed circuit board 103 by adhesive 111 and molding compound 112.

A longstanding and unsolved problem with printed circuit boards in general and with BGA package 100 in particular is that printed circuit board 100 may develop a crack, such as crack 113. Crack 113 destroys the structural integrity of BGA package 100. Once the structural integrity of BGA package 100 is destroyed, unforseen stresses may break or damage electronic connectors, such as electronic connectors 115 and 116, and as a result, any product in which BGA package 100 is incorporated may malfunction.

One method of solving problems associated with printed circuit board cracking and the resulting electronic connection failures is to include a second printed circuit board in the design of an electronic system. The second circuit board is a redundant printed circuit board which mirrors the operation of the primary board, so a system failure occurs only when both the redundant printed circuit board and the primary board fail at the same time. Unfortunately, this solution is very expensive and is cost effective only in systems, such as trains, airplanes, or spacecraft, where the cost of failure is high. For systems in which the cost of failure is low, redundant circuit boards are seldom used.

For these and other reasons there is a need for the present invention.

Summary of the Invention

The above mentioned problems with cracking in circuit boards and other problems are addressed by the present invention and will be understood by reading and studying the following specification. A circuit board is described that includes embedded fibers, which strengthen the board, and a surface layer having a certain thickness range that inhibits the formation of cracks in the circuit board.

The present invention provides, in one embodiment, a circuit board including a core layer and a surface layer. A number of fibers are embedded in the core layer. The surface layer has a thickness which is between about 10% and about 30% of the circuit board thickness. Embedding fibers in the core layer increases the strength of the circuit board. A surface layer thickness of between about 10% and about 30% of the circuit board thickness inhibits the formation of cracks in the circuit board, which improves the reliability of circuits mounted on the circuit board and systems in which the circuit board is embedded.

In an alternate embodiment, the present invention provides a method of fabricating a circuit board having a circuit board thickness. The method includes forming a core layer including a number of fibers, and forming a surface layer on the core layer. The surface layer has a surface layer thickness that is between about 10% and about 30% of the circuit board thickness and is free of fibers.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figure 1 is an illustration cross-sectional view of a prior art ball-grid array (BGA) package including a circuit board.

Figure 2A is a cross-sectional view of one embodiment of a circuit board assembly according to the teaching of the present invention.

Figure 2B is a cross-sectional view of an alternate embodiment of a circuit board assembly according to the teaching of the present invention.

Figure 2C is a cross-sectional view of a second alternate embodiment of a circuit board assembly according to the teaching of the present invention.

Figure 3 is a block diagram of one embodiment of a computer system suitable for use in connection with the present invention.

Detailed Description

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

Figure 2A is a cross-sectional view of one embodiment of circuit board assembly 200. Circuit board assembly 200 includes die 201, printed circuit board 202, and board 203. Circuit board 202 is coupled to board 203 by solder balls 204, and die 201 is coupled to printed circuit board 202 by adhesive 205 and molding compound 206.

Circuit board assembly 200 is sometimes referred to as a ball-grid array, but the present invention is not limited to ball-grid array circuit board assemblies. Any circuit board assembly that includes a circuit board, such as printed circuit board 202, which is described in more detail below, is suitable for use in connection with the present invention. For example, a circuit board assembly in which a first circuit board is coupled by edge connectors to a second circuit board is suitable for use in connection with the present invention.

Die 201 includes an integrated circuit, such as a memory circuit, a processor, an amplifier, or an application specific circuit (ASIC). Memory circuits suitable for use in connection with the present invention include but are not limited to dynamic random access memory (DRAM) circuits, static random access memory (SRAM) circuits, erasable programmable memory (EPROM) circuits, and electrically erasable programmable memory (EEPROM) circuits. Processor circuits suitable for use in connection with the present invention include but are not limited to microprocessors, digital signal processors (DSPs), and reduced instruction set computing (RISC) processors. Amplifier circuits suitable for use in connection with the present invention include but are not limited to operational amplifiers, differential amplifiers, and power amplifiers. Application specific integrated circuits (ASICs) suitable for use in connection with the present invention include telecommunication circuits, such as telecommunication interface circuits. Die 201 is coupled to printed circuit board 202 by adhesive 205, which is selected to maintain a low stress interface between die 201 and circuit board 202. Any adhesive that has a coefficient of thermal expansion which maintains a low stress interface between die 201 and circuit board 202 during the heating and cooling of circuit board assembly 200 is suitable for use in connection with the present invention.

A board 203, such as a circuit board, provides a substrate for mounting a number of circuit boards, such as circuit board 202, and other electronic or electro-mechanical components. In one embodiment, board 203 is a computer system circuit board including a processor. Board 203 may also provide a substrate suitable for securing circuit assembly 200 to a larger package or other housing, such as a cabinet or case. Board 203 is fabricated from materials commonly used in the fabrication of circuit boards, such as polymeric composite materials. One example of a polymeric composite material is phenolic. However, board 203 is not limited to polymeric composite materials, and other materials, particularly insulating materials, may also be used in the fabrication of board 203.

Solder balls 204 provide a number of signal paths to electronically couple circuit board 202 to board 203. The number of signal paths permit communication between

components mounted on circuit board 202 and on board 203. Any material that is a good conductor is suitable for use in fabricating solder balls 204. Tin, gold, copper, silver, and alloys of tin, gold, copper, and silver, are examples of materials suitable for use fabricating solder balls 204.

Circuit board 202, as shown in Figure 2A, provides a substrate for mounting die 201 and coupling signals to board 203. In one embodiment, circuit board 202 is formed from a polymeric composite material. Circuit board 202 is coupled to die 201 by adhesive 205.

Figure 2B is a detailed cross-sectional view of one embodiment of circuit board 202. In this embodiment, circuit board 202 includes core layer 208 and surface layer 209, which is a first layer or a first resin layer. Circuit board 202 may also include slot 211 for routing conductive connectors, such as conductive connectors 207 and 208 shown in Figure 2A, from above circuit board 202 to below circuit board 202.

Core layer 208 includes one or more fibers 213 embedded in an insulator. Core layer 208, in one embodiment, is fabricated from a resin and has a thickness 212 of between about .006 inches and about .012 inches. The one or more fibers 213, in one embodiment, are glass fibers having a diameter of between about .0005 inches and about .001 inches. In an alternate embodiment, the one or more fibers 213 are woven fibers, such as woven glass fibers, and have a diameter of between about .001 inches and about .002 inches.

Surface layer 209, in one embodiment, is fabricated from a resin that is free of fibers. In an alternate embodiment, surface layer 209 is fabricated from a resin that is essentially free of fibers. Surface layer 209 is essentially free of fibers when any fibers embedded in surface layer 209 do not significantly increase the likelihood of cracking in circuit board 202. The inventors discovered that cracks in circuit board 202 frequently occur on the surface of circuit board 202 at stress concentration points located above fiber hills, such as fiber hills 215 and 217, and that cracks are less likely to occur at stress concentration points located above fiber valleys. In board assembly 200, stress concentration points occur along an edge of an interface between two surfaces, such as along the edge of adhesive 205 at the interface between adhesive 205 and circuit board

202, as shown in Figure 2A. The inventors also discovered that cracks at stress concentration points were most likely to occur during the solder reflow process, when temperature gradients are formed in board assembly 200. Once a surface crack, such as surface crack 219 intersects with a fiber, such as the one or more fibers 213, the crack proceeds along the interfacial interface between the one or more fibers 213 and the material in which the one or more fibers 213 is embedded. According to the teachings of the present invention, the inventors also discovered that by increasing thickness 210 of surface layer 209 to between about 10% and 30% of circuit board thickness 221, the likelihood of crack formation on the surface of circuit board 202 is decreased. Therefore, in the novel circuit board of the present invention, the thickness 210 is preferably between about 10% and about 30% of circuit board thickness 221.

Figure 2C is a detailed cross-sectional view of an alternate embodiment of circuit board 202. In this embodiment, circuit board 202 includes core layer 223, first surface layer 225, and second surface layer 227. Core layer 223 is located between first surface layer 225 and second surface layer 227.

Core layer 223 includes one or more fibers 231 embedded in core layer 223. Core layer 223, in one embodiment, is fabricated from a resin and has a thickness 229 of between about .006 inches and about .012 inches. Core layer 223 also has greater mechanical strength than first surface layer 225 or second surface layer 227. The one or more fibers 231, in one embodiment, embedded in core layer 223, are glass fibers having a diameter of between about .0005 inches and about .001 inches. In an alternate embodiment, the one or more fibers 231 are woven fibers, such as woven glass fibers, and have a diameter of between about .001 inches and about .002 inches.

First and second surface layers 225 and 227, in one embodiment, are fabricated from a resin that is free of fibers. In an alternate embodiment, first and second surface layers 225 and 227 are fabricated from a resin that is essentially free of fibers. First and second surface layers 225 and 227 are essentially free of fibers when any fibers embedded in first and second surface layers 225 and 227 do not significantly increase the likelihood of cracking in circuit board 202. The inventors, in addition to discovering the source of cracks in circuit boards having a single surface layer, have also discovered that cracks in

a circuit board having two surface layers, such as circuit board 202 shown in Figure 2C, frequently occur on one of the surfaces of circuit board 202 at stress concentration points located above fiber hills, such as fiber hills 233 and 235, and that cracks are less likely to occur at stress concentration points located above fiber valleys. In board assembly 200, which is shown in Figure 2A, stress concentration points occur along an edge of an interface between two surfaces, such as along the edge of adhesive 205 at the interface between adhesive 205 and circuit board 202. The inventors also discovered that cracks at stress concentration points were most likely to occur during the solder reflow process when temperature gradients are being formed in board assembly 200. Referring again to figure 2C, once a surface crack intersects a fiber, such as one of the number of fibers 231, the crack proceeds along the interfacial interface between one of the number of fibers 231 and the material in which one of the number of fibers 235 is embedded. The inventors also discovered that by increasing the thickness 237 of surface layer 225 to between about 10% and 15% of circuit board thickness 241 and the thickness 239 of surface layer 227 to between about 10% and 15% of circuit board thickness 241, the likelihood of crack formation on the surface of circuit board 202 is decreased. Therefore, first surface layer thickness 237 is preferably between about 10% and about 15% of circuit board thickness 241 and second surface layer thickness 239 are preferably between about 10% and about 15% of circuit board thickness 241.

Figure 3 is a block diagram of one embodiment of a computer system 300 suitable for use in connection with the present invention. System 300 comprises processor 305 and memory board assembly 310 including one or more circuit boards shown in Figures 2B and 2C according to the teachings of the present invention. Memory board assembly 310 comprises memory array 315, address circuitry 320, and read circuitry 330, and is coupled to processor 305 by address bus 335, data bus 340, and control bus 345. Processor 305, through address bus 335, data bus 340, and control bus 345 communicates with memory board assembly 310. In a read operation initiated by processor 305, address information, data information, and control information are provided to memory board assembly 310 through busses 335, 340, and 345. This information is decoded by addressing circuitry 320, including a row decoder and a column decoder, and read

circuitry 330. Successful completion of the read operation results in information from memory array 315 being communicated to processor 305 over data bus 340.

Conclusion

A number of circuit boards, circuit board assemblies, and methods of fabricating circuit boards and circuit board assemblies have been described. The circuit boards include a number of layers including a core layer and one or more surface layers. The core layer includes a number of embedded fibers to increase the strength of the core layer. Cracking is reduced in the surface layer or layers by fabricating the surface layers with a thickness sufficient to reduce the probability of stress concentration points inducing cracks during the heating and cooling of the circuit board. The methods described for fabricating a circuit board include forming a core layer including a number of fibers, and forming a surface layer on the core layer, such that the surface layer is free of fibers and has thickness that is between about 10% and 30% of the circuit board thickness. Cracking is reduced in the surface layer or layers of circuit boards fabricated using the methods of the present invention.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A circuit board having a circuit board thickness, the circuit board comprising:

a core layer including one or more fibers; and

a surface layer having a surface layer thickness that is between about 10% and about 30% of the circuit board thickness, the surface layer being free of fibers.

2. The circuit board of claim 1, wherein the core layer is fabricated from a resin in which the one or more fibers are embedded.

3. The circuit board of claim 1, wherein at least one of the one or more fibers comprises a glass fiber.

4. A circuit board having a circuit board thickness, the circuit board comprising:

a core layer including a number of fibers; and

a surface resin layer having a surface layer thickness that is between about 10% and about 30% of the circuit board thickness.

5. The circuit board of claim 4, wherein the core layer is a polymeric composite material.

6. The circuit board of claim 4, wherein the core layer has a thickness of between about .006 inches and .012 inches.

7. A circuit board having a circuit board thickness, the circuit board comprising:

a first layer having a first layer thickness that is between about 10% to 15% of the circuit board thickness, the first layer being free of fibers;

a second layer having a second layer thickness that is between about 10% to 15% of the circuit board thickness; and

a core layer located between the first layer and the second layer, the core layer including a number of fibers.

8. The circuit board of claim 7, wherein the core layer has greater mechanical strength that the first layer.

9. The circuit board of claim 7, wherein the core layer has greater mechanical strength that the second layer.

10. A circuit board having a circuit board thickness, the circuit board comprising:

a first resin layer having a first layer thickness that is between about 10% and about 15% of the circuit board thickness;

a second resin layer having a second layer thickness that is between about 10% and about 15% of the circuit board thickness; and

a core layer located between the first resin layer and the second resin layer, the core layer including a number of fibers.

11. The circuit board of claim 10, wherein the first resin layer is free of fibers.

12. The circuit board of claim 11, wherein the second resin layer is free of fibers.

13. A circuit board assembly comprising:

a first circuit board;

a second circuit board coupled to the first circuit board, the second circuit board having a thickness and including a number of fibers having a fiber thickness of between about .001 inches and about .002 inches, the second circuit board having a surface located at a distance of between about 10 % to 20% of the thickness away from the number of fibers; and

a die coupled to the second circuit board.

14. The circuit board assembly of claim 13, wherein the die includes a dynamic random access memory (DRAM).

15. The circuit board assembly of claim 13, wherein the die includes a processor.

16. A circuit board assembly comprising:

a first circuit board;

a second circuit board coupled to the first circuit board, the second circuit board having a thickness and including a number of fibers having a fiber thickness of between about .001 inches and about .002 inches, the second circuit board having a surface located at a distance of between about 10 % and about 30% of the thickness away from the number of fibers; and

a die coupled to the second circuit board.

17. The circuit board assembly of claim 16, wherein the die includes an amplifier.

18. The circuit board assembly of claim 16, wherein the die includes an application specific integrated circuit (ASIC).

19. A circuit board assembly comprising:

a first circuit board;

a second circuit board coupled to the first circuit board, the second circuit board comprising:

a core layer including a number of fibers; and

a surface layer having a surface layer thickness that is between about 10% and about 30% of the circuit board thickness, the surface layer being free of fibers; and

a die coupled to the second circuit board.

20. The circuit board assembly of claim 19, wherein the second circuit board has a thickness and includes a number of fibers having a fiber thickness of between about .001

inches and about .002 inches, the second circuit board has a surface located at a distance of between about 10% and 30% of the thickness away from the number of fibers.

21. A circuit board assembly comprising:

a first circuit board;

a second circuit board coupled to the first circuit board, the second circuit board having a thickness and including a number of fibers having a fiber thickness of between about .001 inches and about .002 inches, the second circuit board having a first surface located at a first distance of between about 10 % to 15% of the thickness away from the number of fibers and a second surface located at a second distance of between about 10% to 15% of the thickness away from the number of fibers; and

a die coupled to the second circuit board.

22. The circuit board assembly of claim 21, wherein the first circuit board is a computer system circuit board.

23. The circuit board assembly of claim 21, wherein the second circuit board is a memory circuit board.

24. A circuit board assembly comprising:

a first circuit board;

a second circuit board coupled to the first circuit board, the second circuit board having a thickness, the second circuit board having a first surface located at a first distance of between about 10 % and about 15% of the thickness away from a number of fibers and a second surface located at a second distance of between about 10% and about 15% of the thickness away from the number of fibers; and

a die coupled to the second circuit board.

25. The circuit board assembly of claim 24, wherein the die is coupled to the second circuit board by an adhesive.

26. A system comprising:

a processor;

a die having a number of memory circuits, at least one of the number of memory circuits being coupled to the processor; and

a circuit board coupled to the die, the circuit board having a surface and a thickness, and the circuit board including a number of embedded fibers such that the number of embedded fibers are located at a distance of between about 10% to 30% from the surface of the circuit board.

27. The system of claim 26, wherein the processor is a microprocessor.

28. The system of claim 26, wherein the number of memory circuits are static random access memory (SRAM) circuits.

29. A system comprising:

a processor;

a die having a number of memory circuits, at least one of the number of memory circuits being coupled to the processor; and

a circuit board coupled to the die, the circuit board having a first surface, a second surface, and a thickness, and the circuit board including a number of embedded fibers such that the number of embedded fibers are located at a distance of between about 10% and about 15% from the first surface and at a distance of between about 10% and about 15% from the second surface.

30. The system of claim 29, wherein the processor is a reduced instruction set computer (RISC).

31. The system of claim 29, wherein the number of embedded fibers is one.

32. A system comprising:

a processor;

a die having a number of memory circuits, at least one of the number of memory circuits being coupled to the processor; and

a circuit board coupled to the die, the circuit board having a first surface, a second surface, and a thickness, and the circuit board including a number of embedded fibers, each of the number of embedded fibers having a thickness of between about .010 inches and .020 inches, the number of embedded fibers are located at a distance of between about 10% to 15% from the first surface and at a distance of between about 10% to 15% from the second surface.

33. The system of claim 32, wherein the processor is a digital signal processor (DSP).

34. The system of claim 32, wherein the circuit board is thermally coupled to the die.

35. A method of fabricating a circuit board having a circuit board thickness, the method comprising:

forming a core layer including a number of fibers; and

forming a surface layer on the core layer, the surface layer having a surface layer thickness that is between about 10% and about 30% of the circuit board thickness, the surface layer being free of fibers.

36. The method of claim 35, wherein forming a core layer including a number of fibers comprises:

embedding the number of fibers in a resin.

37. The method of claim 35, wherein forming a core layer including a number of fibers comprises:

embedding the number of fibers in a polymeric composite material.

38. A method of fabricating a circuit board having a circuit board thickness, the method comprising:

forming a core layer including a number of fibers; and

forming a surface resin layer on the core layer, the surface layer having a surface layer thickness that is between about 10% to 30% of the circuit board thickness.

39. The method of claim 38, further comprising:

forming a number of slots in the circuit board.

40. The method of claim 38, further comprising:

mounting a die using an adhesive over each of the number of slots.

41. A method of fabricating a circuit board having a circuit board thickness comprising:

forming a core layer including a number of fibers;

forming a first layer on the core layer, the first layer having a thickness between about 10% and about 15% of the circuit board thickness and the first layer being free of fibers; and

forming a second layer on the core layer, the second having a thickness that is between about 10% and about 15% of the circuit board thickness.

42. A method of fabricating a circuit board having a circuit board thickness comprising:

forming a core layer including a number of fibers;

forming a first layer on a first side of the core layer, the first layer having a thickness between about 10% and about 15% of the circuit board thickness and the first layer being free of fibers; and

forming a second layer on a second side of the core layer, the second having a thickness that is between about 10% and about 15% of the circuit board thickness.

43. A method of fabricating a circuit board having a circuit board thickness comprising:

forming a core layer including a number of fibers;

forming a first resin layer on the core layer, the first resin layer having a thickness between about 10% and about 15% of the circuit board thickness; and

forming a second resin layer on the core layer, the second resin layer having a thickness that is between about 10% and about 15% of the circuit board thickness.

44. The method of claim 43, wherein forming the core layer includes embedding the fibers in a resin layer.

Abstract

This invention relates to circuit boards and methods of fabricating circuit boards. A circuit board includes a core layer and a surface layer. The core layer includes a number of fibers and the surface layer has a thickness that is between about 10% and about 30% of the circuit board thickness. Including fibers in the core layer increases the strength of the circuit board. The surface layer is essentially free of fibers and relatively thick. The thickness of the surface layer inhibits the formation of cracks in the circuit board, which improves the reliability of circuits and systems coupled to the circuit board.

"Express Mail" mailing label number: EL600375937US
Date of Deposit: August 22, 2000
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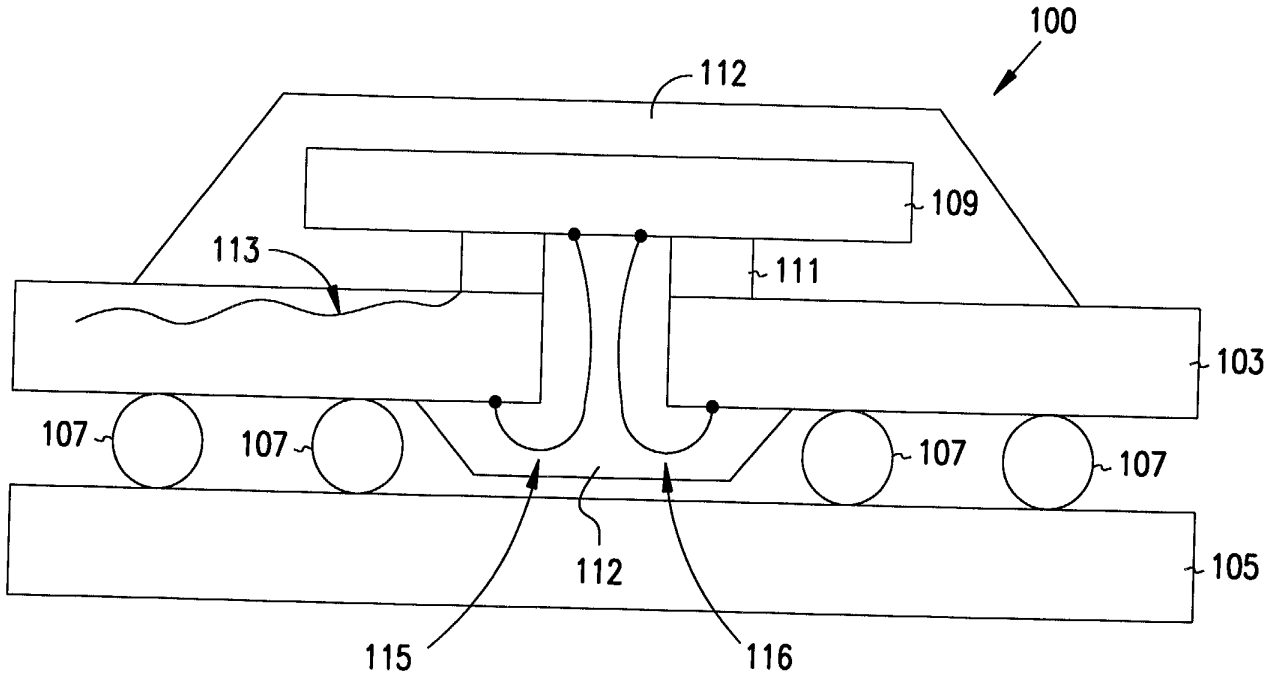

Figure 1
(PRIOR ART)

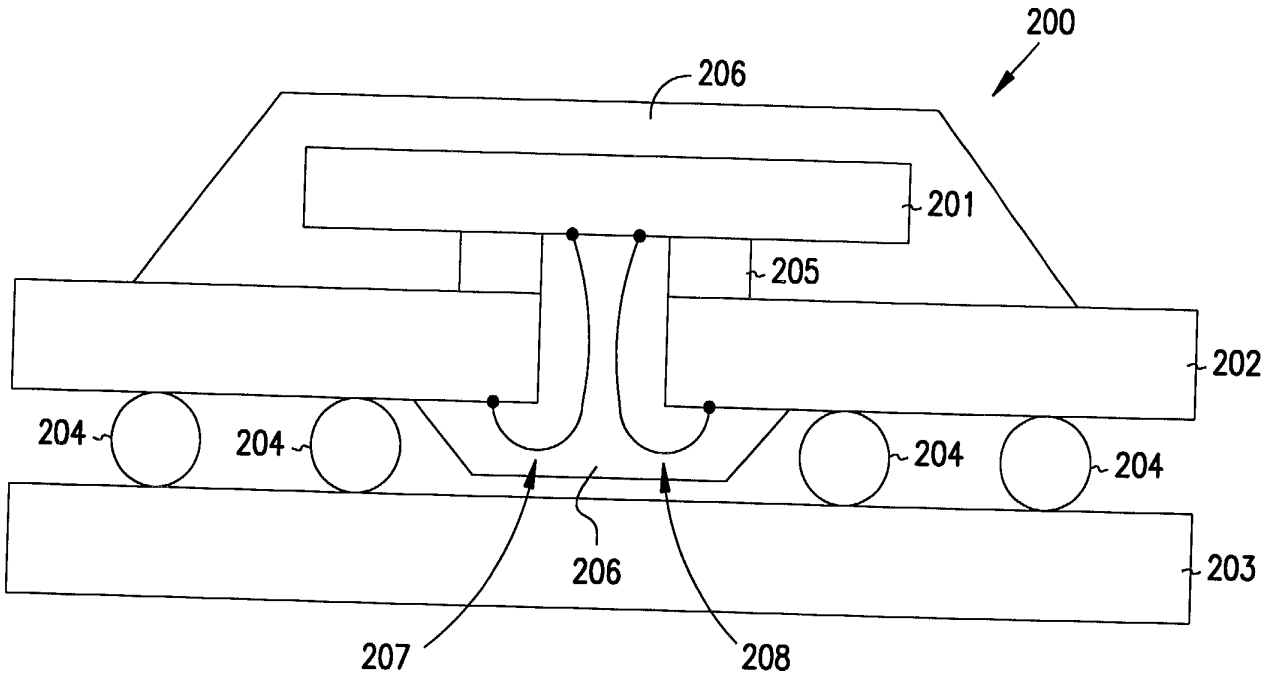

Figure 2A

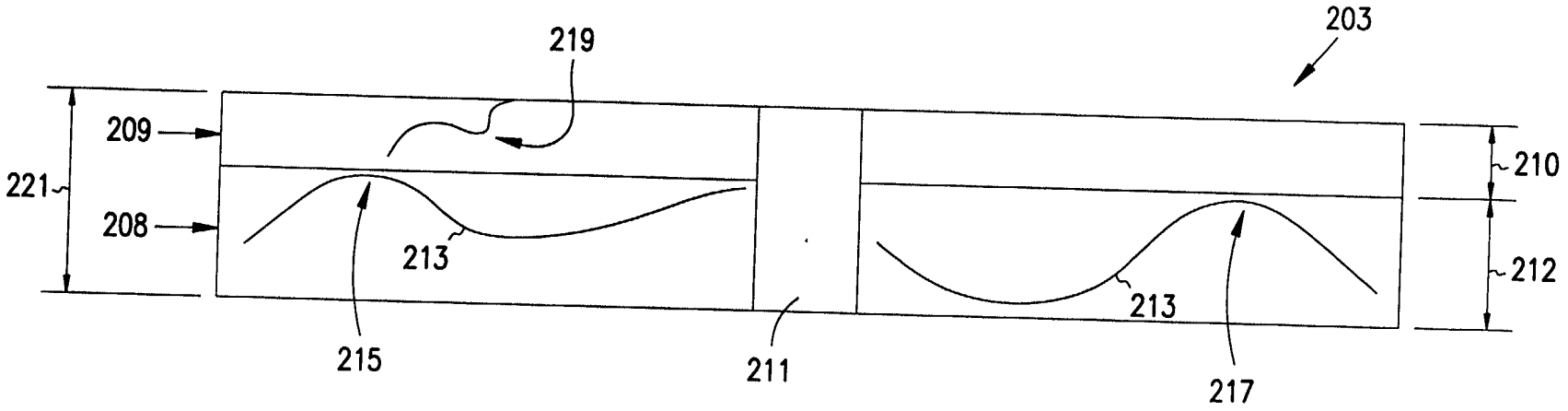

Figure 2B

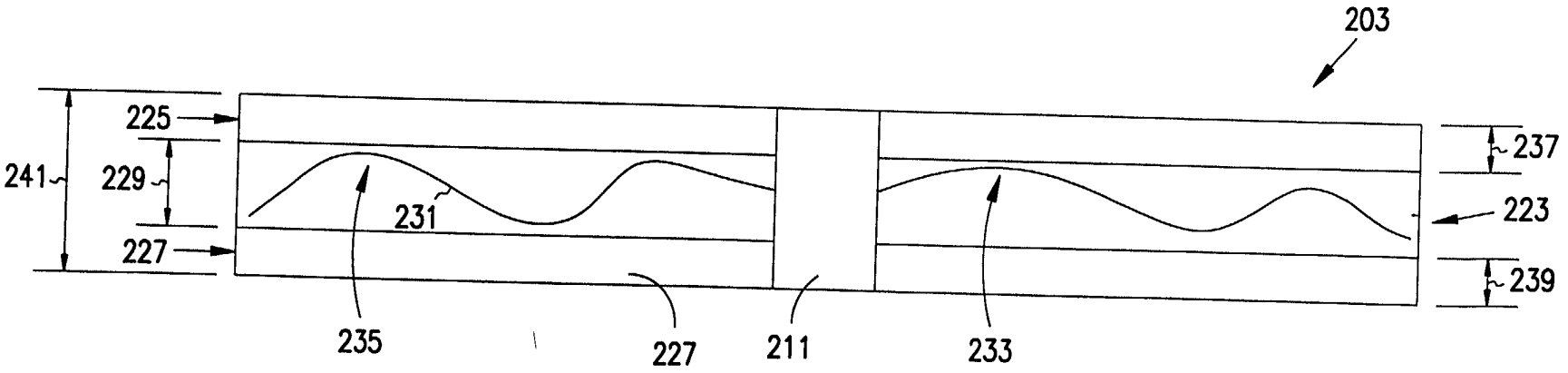

Figure 2C

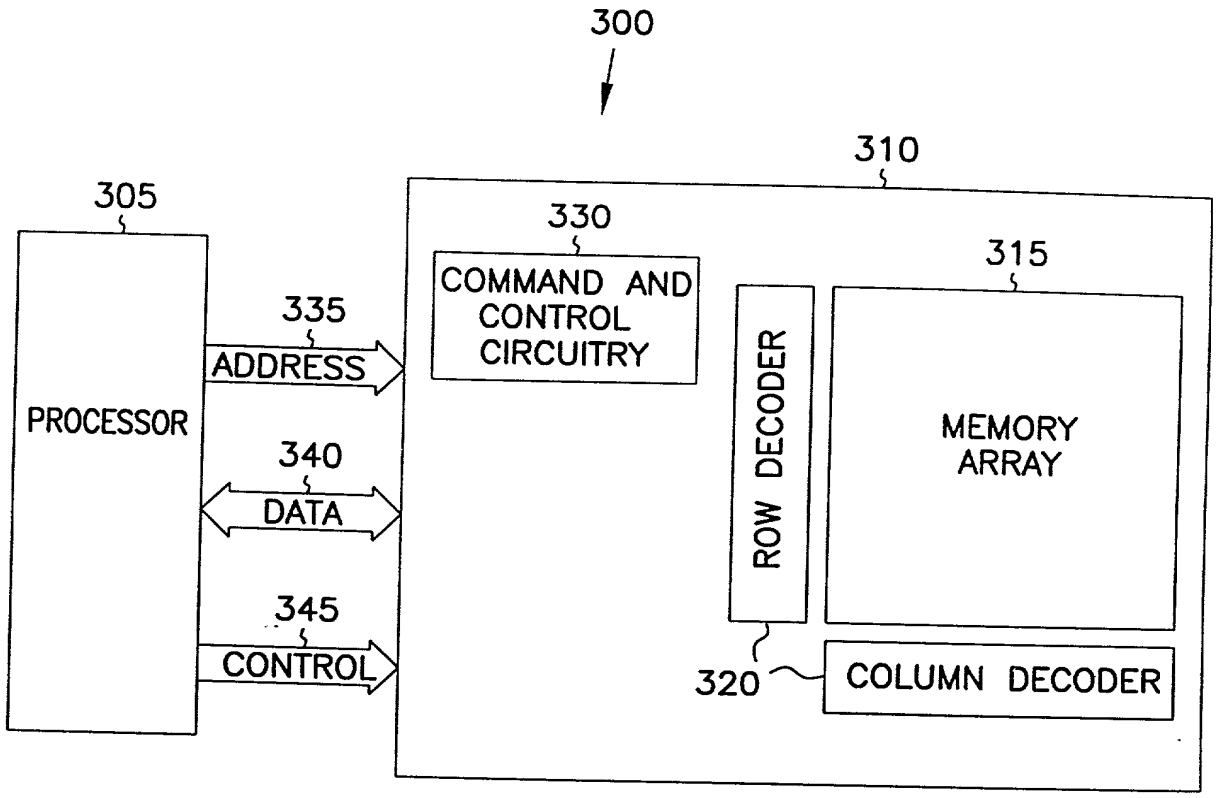
300
310
305
330
315
COMMAND AND CONTROL CIRCUITRY
335
ADDRESS
PROCESSOR
340
DATA
345
CONTROL
ROW DECODER
MEMORY ARRAY
320
COLUMN DECODER

Figure 3

SCHWEGMAN ■ LUNDBERG ■ WOESSNER ■ KLUTH

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first an joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CIRCUIT BOARD .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Signature: _____ Date: 8/22/00
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#159
Boise, ID 83706

Signature: _____ Date: 08/22/00
Yong Du

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.